Silicon Research at Intel

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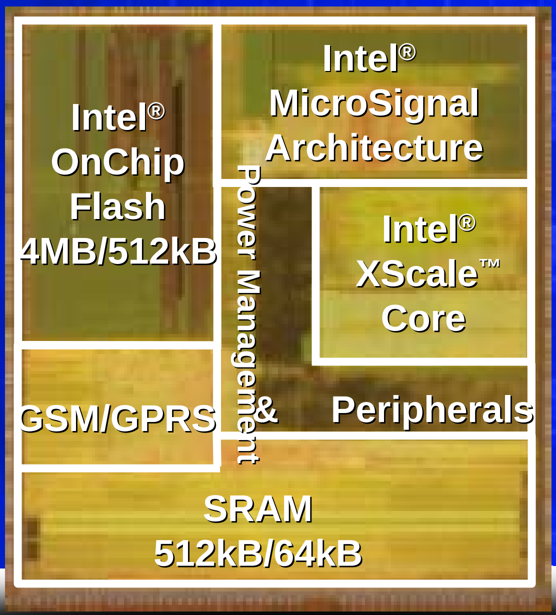
Technology and Manufacturing Group
Hillsboro, Oregon

March 6, 2004

Entering A New Era

Convergence
Higher level of Product Integration

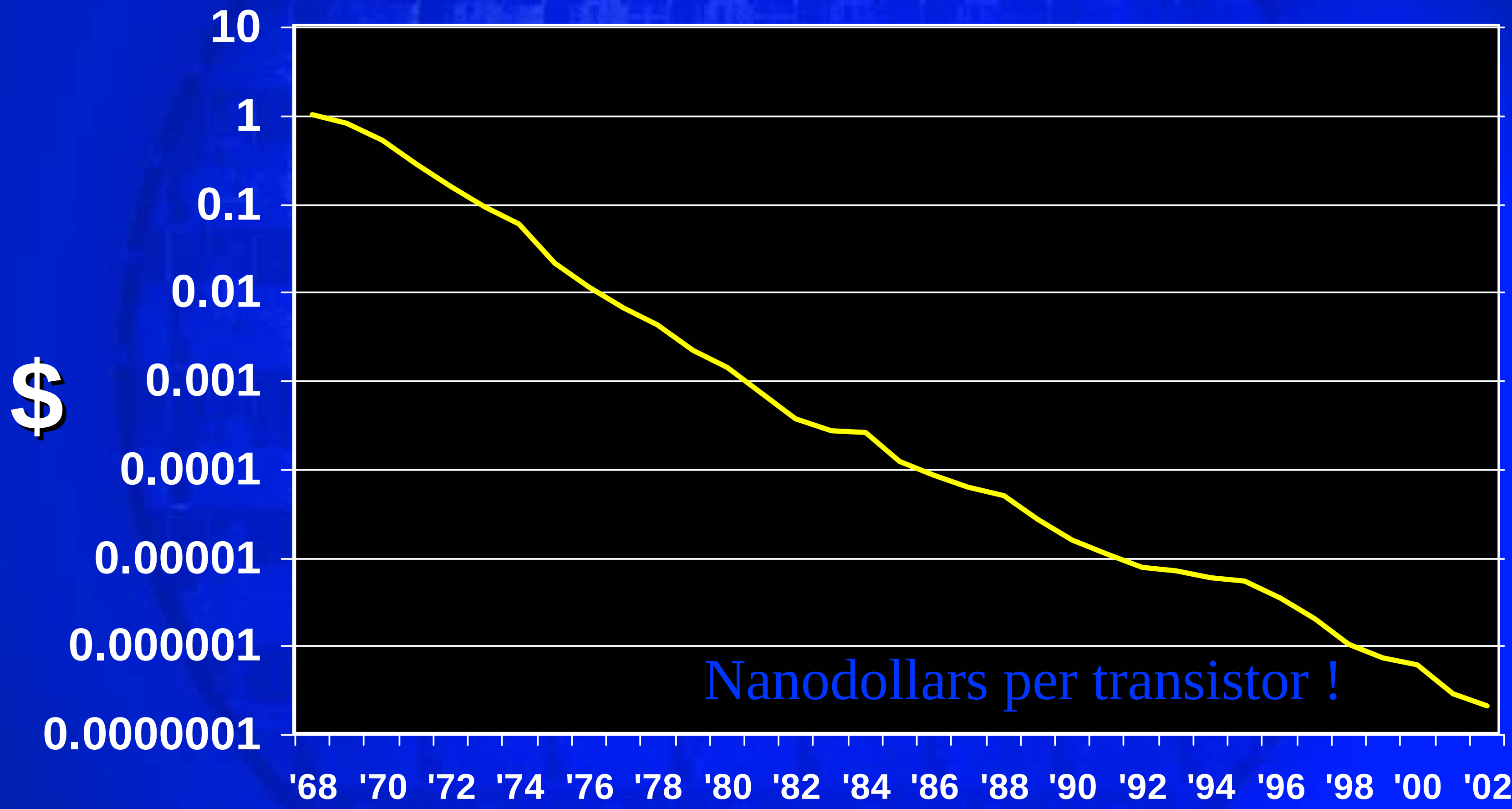


Intel® PXA800F Processor

Intel® Mobile Technology

Moore's Law Scaling

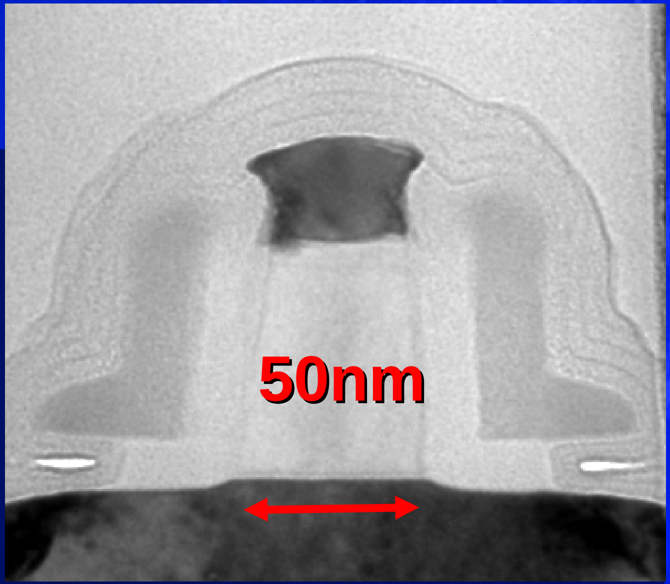
Nearly 7 Orders Of Magnitude Reduction in Cost/Transistor



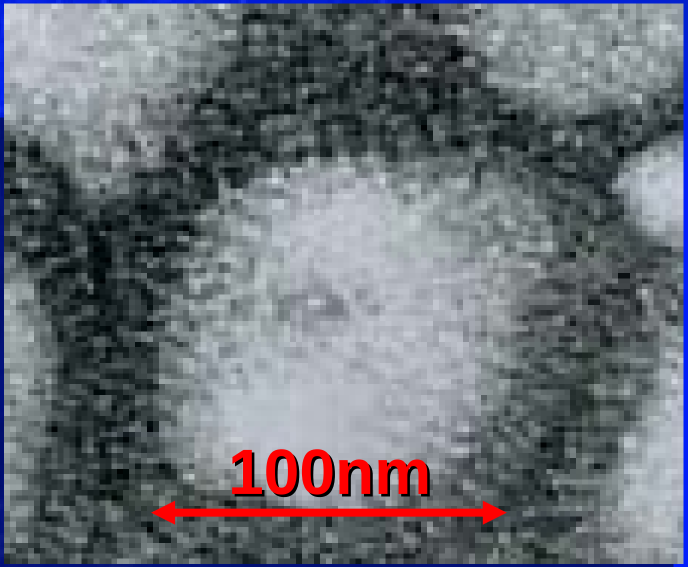
Source: WSTS/Dataquest/Intel, 8/02

Moore's Law in Action

Nanotechnology is production today !



Transistor for 90nm-node
Gate oxide=1.2nm
Source: Intel



Influenza virus
Source: CDC

Intel's 90nm node transistor

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Moore's Law Challenges Going Forward

- Transistor scaling/power
- Lithography optical extension/EUV
- Integration of Ultra-low k
- Metal Line Resistance

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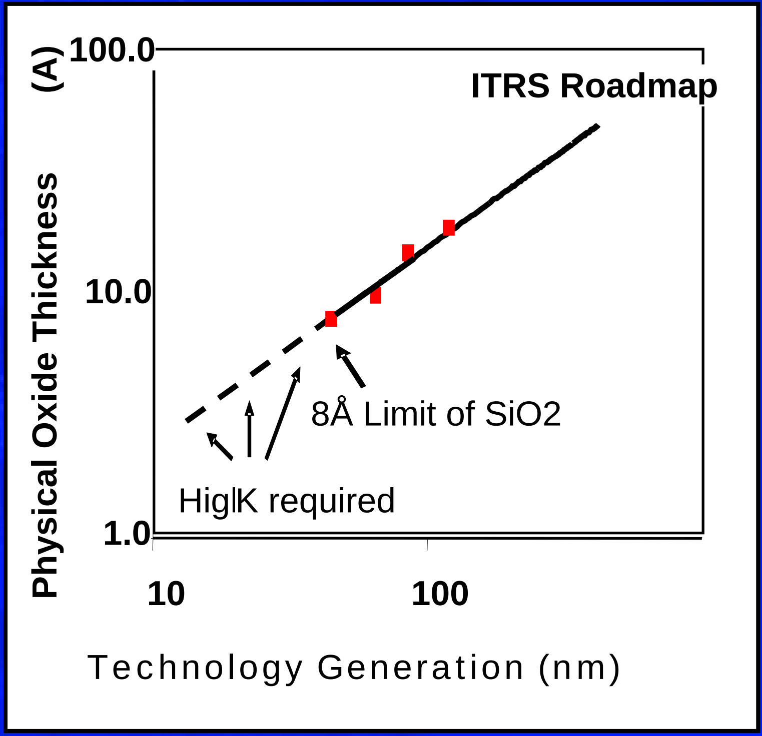
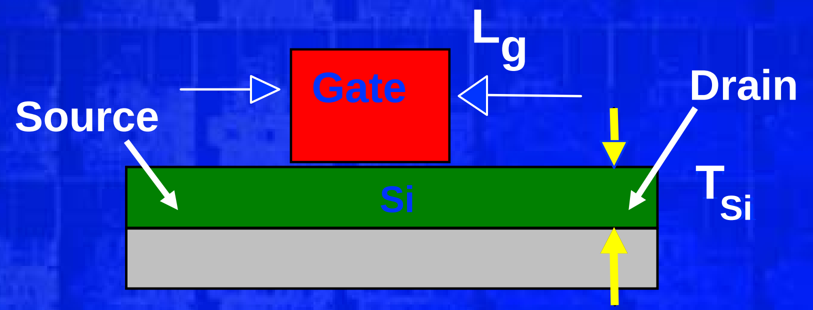
Transistor Power Reduction

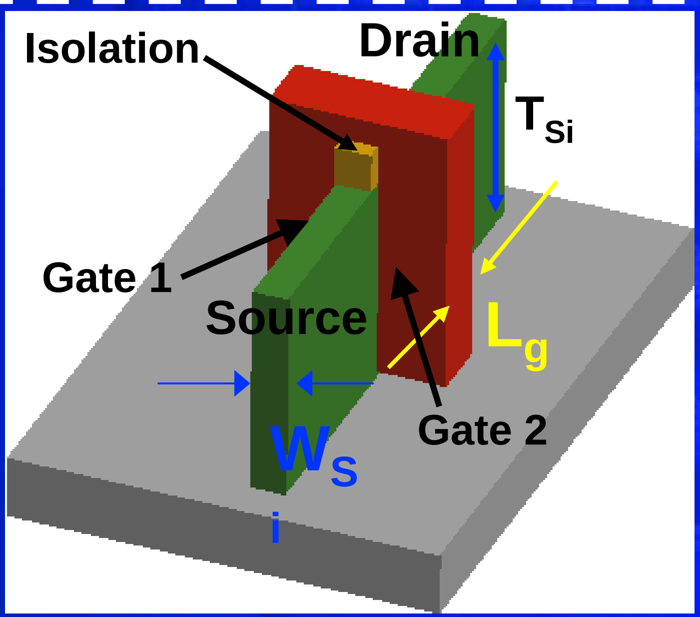
- **Transistor off-state leakage is increasing with decreasing physical L_G**
- **Gate oxide leakage is increasing with reducing thickness**
- **Gate leakage with SiO2 is quantum tunneling limited**
- **New materials are required to overcome obstacles**



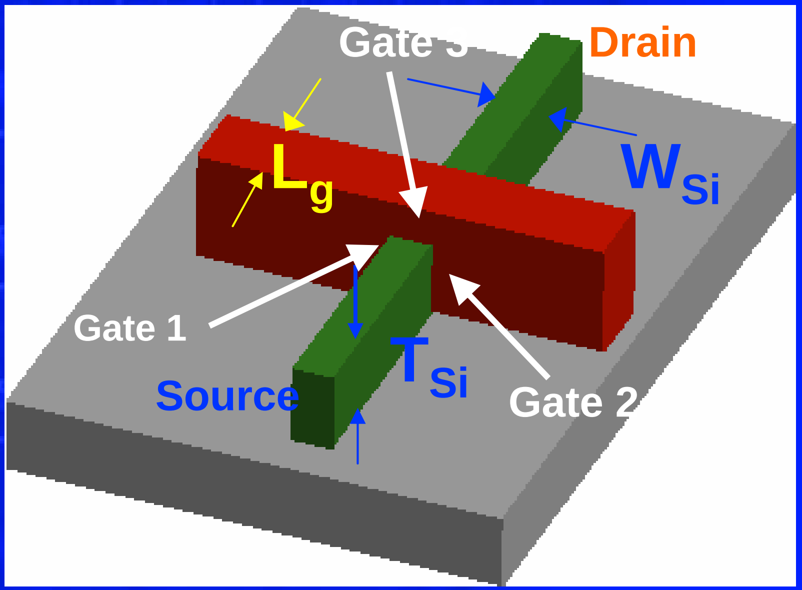
New Transistor Architectures



(Planar)



Double-gate (e.g. FINFET)
(Non-Planar)



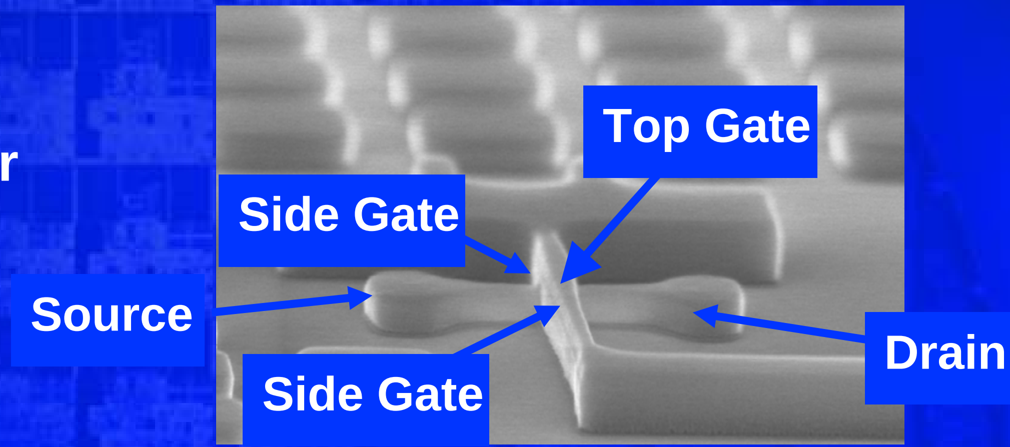
Tri-gate
(Non-Planar)

Source: Intel

Tri-Gate Transistor

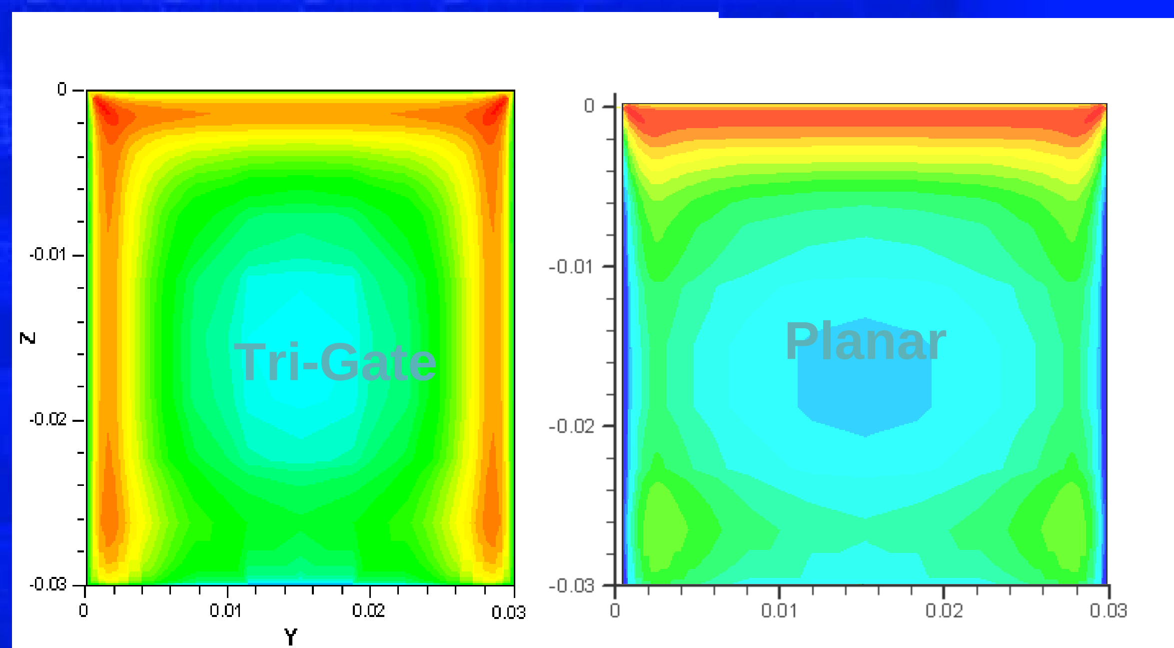
Actual photo

30nm tri-gate transistor



Simulation

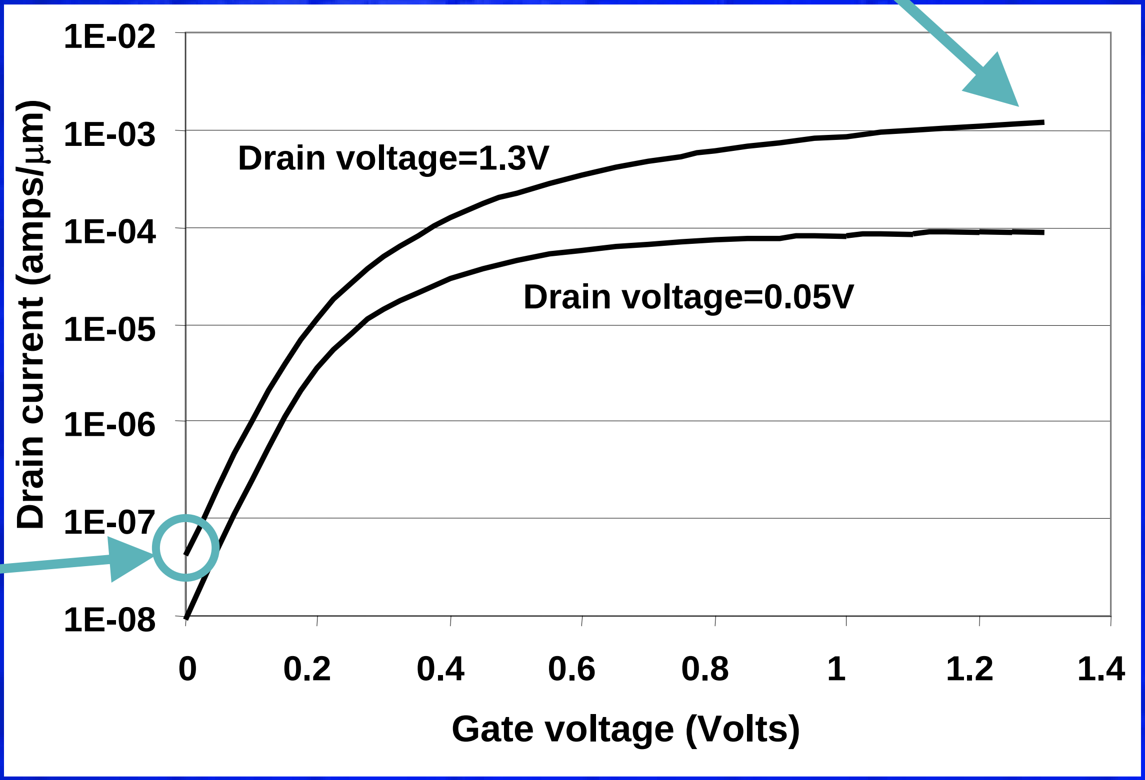
Cross-section of silicon channel shows much more current flow (indicated by red) in tri-gate transistor than in planar transistor



Source: Intel

World Record Non-Planar Performance

Very high drive current at saturation, 1.23 mA/μm



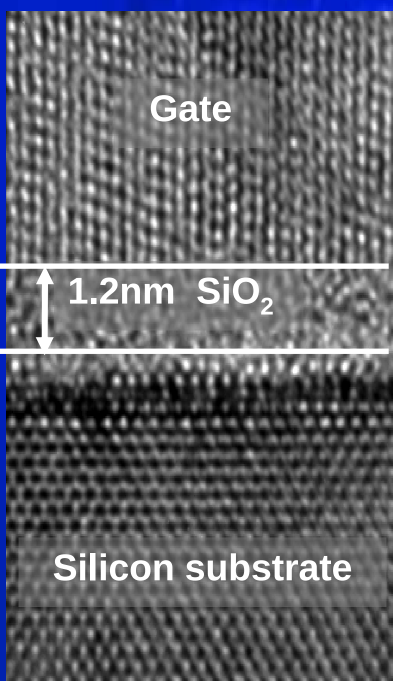
Very low leakage, 40nA/μm

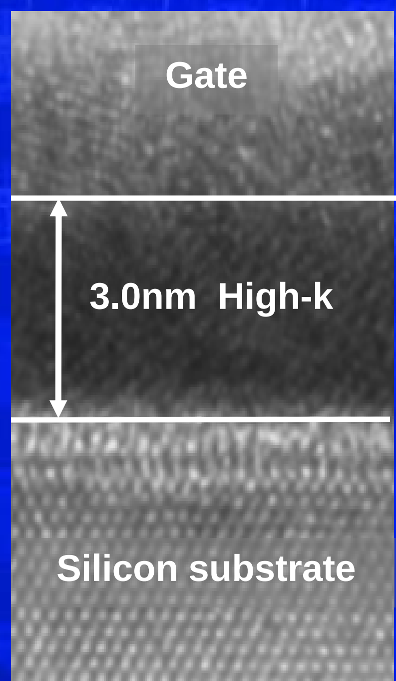
Source: Intel

Tri-gate transistor exhibits excellent device characteristics

High K / Metal Gate Development

- **High-K / metal gate targeted as an option for the 45nm node (1266)**
- **High-K / metal-gate will allow transistor scaling and Moore's Law to continue, and widen Intel's lead in transistor technology**

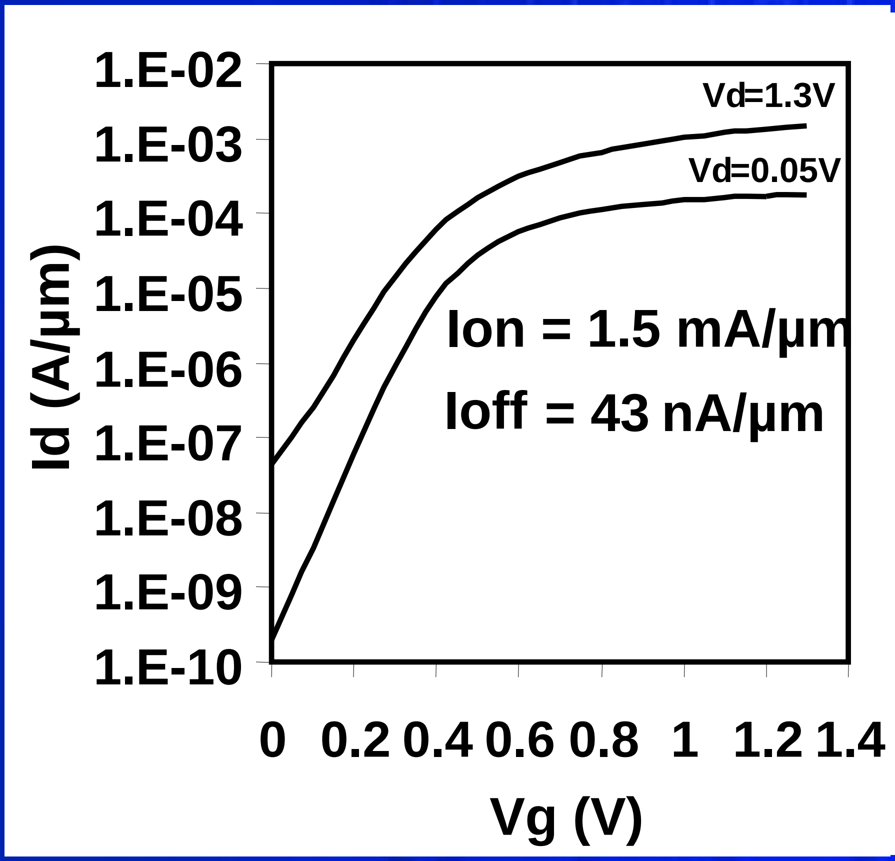


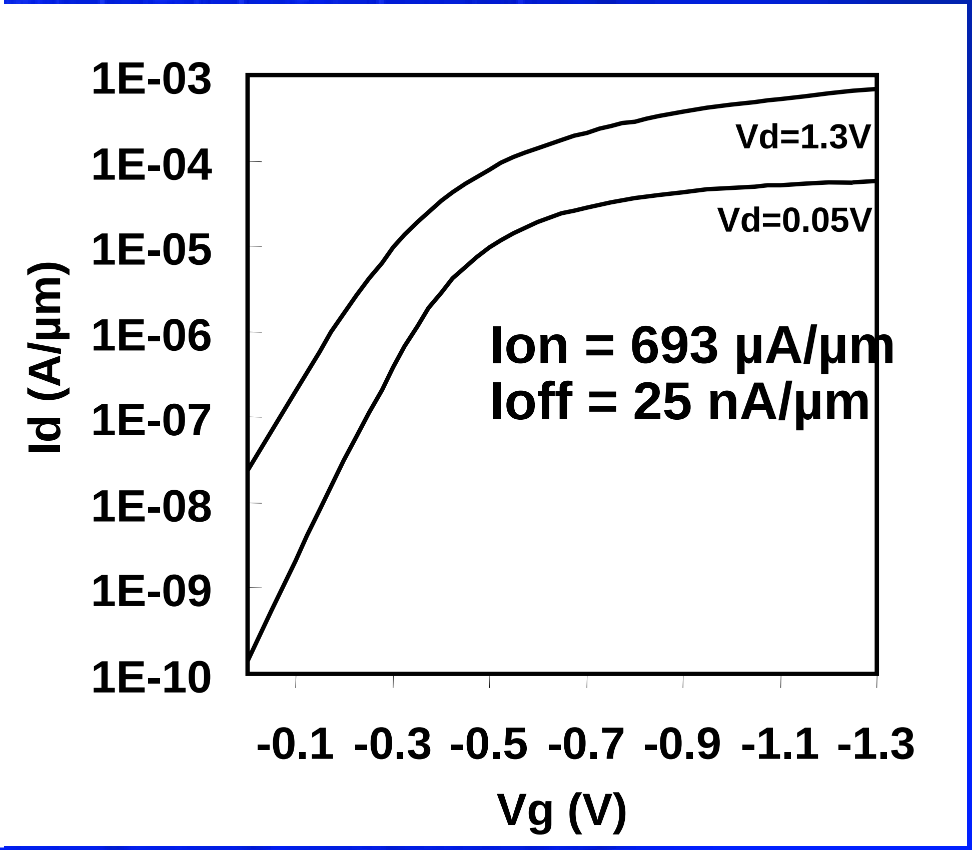


	90nm process	High-k
Capacitance:	**1.0x**	**1.6x**
Leakage:	**1.0x**	**< 0.01x**

Source: Intel

High-K/Metal-Gate Record Setting Performance

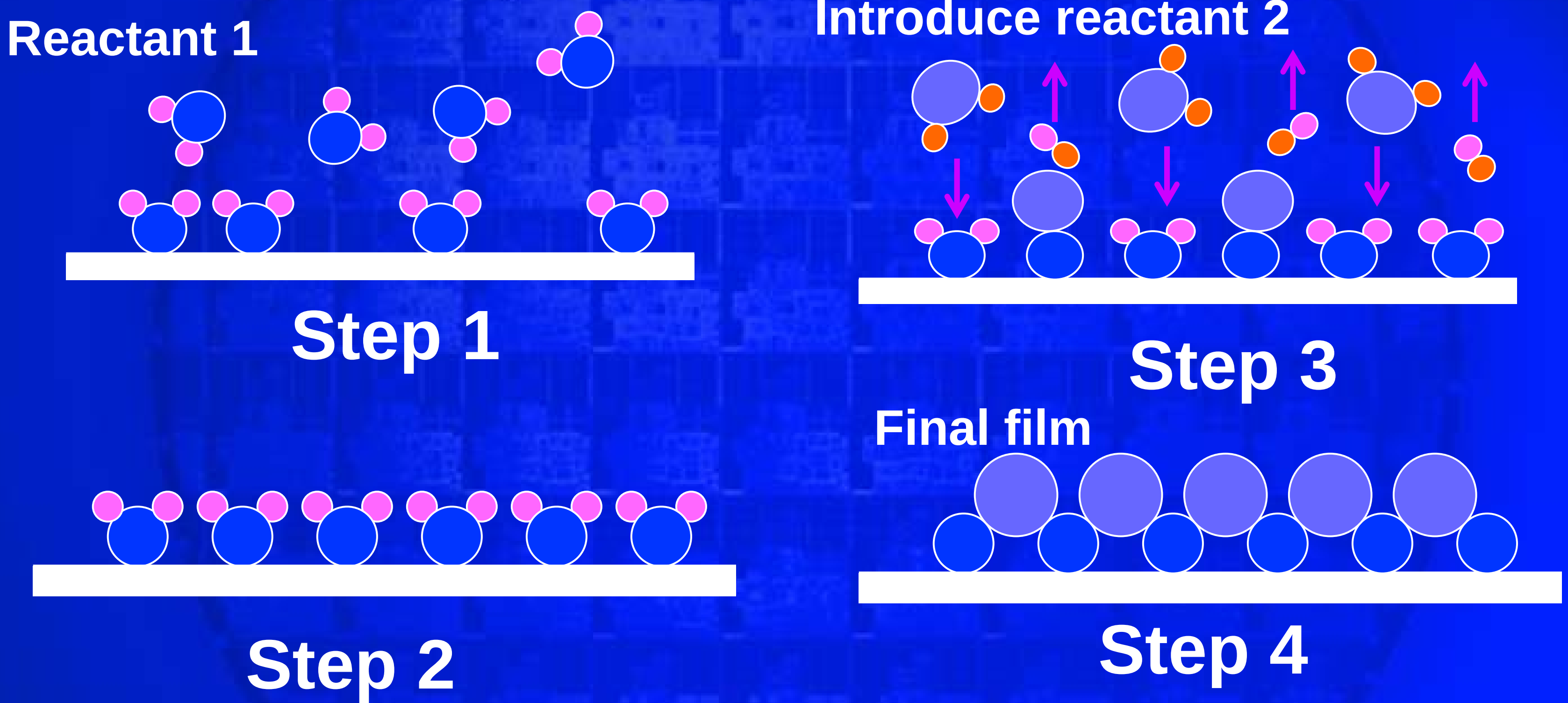




NMOS Transistor **PMOS Transistor**

Source: Intel

High-K Gate Dielectric Formation Atomic Layer Deposition

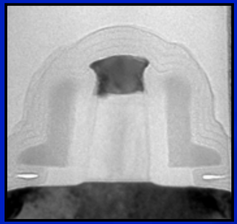


- Sequential introduction of precursors molecules
- Allows for precise building of the dielectric film

Source: Intel

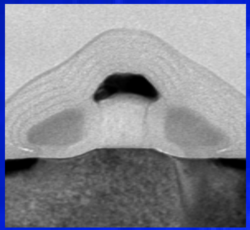
CMOS Device Scaling Demonstration

90nm Node 2003



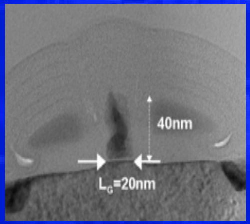
50nm Length (IEDM2002)

65nm Node 2005



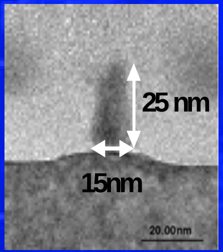
30nm Prototype (IEDM2000)

45nm Node 2007



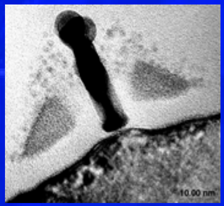
20nm Prototype (VLSI2001)

32nm Node 2009



15nm Prototype (IEDM2001)

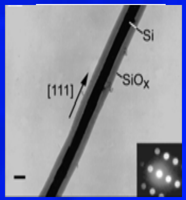
22nm Node 2011



10nm Prototype (DRC 2003)

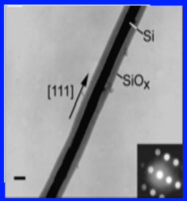
16 nm node 2013

11nm node 2015



TBD

8 nm node 2017



TBD

Intel research devices scale to 10nm (16nm node) Channel engineering solutions (Nanowires/Nanotubes) are being investigated to extend device scaling through end of next decade

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*Source: Intel; Morales and Lieber Science, **279**, 208, 1998*

Novel Devices
What are we looking for?

- Required characteristics:
  - Scalability
  - Performance
  - Energy efficiency
  - Gain
  - Operational reliability
  - Room temp. operation
- Preferred approach:
  - CMOS process compatibility
  - CMOS architectural compatibility

Alternative state variables

- **Spin–electron, nuclear, photon**
- **Phase**
- **Quantum state**
- **Magnetic flux quanta**
- **Mechanical deformation**
- **Dipole orientation**
- **Molecular state**

External Research → Internal Research by end of this decade

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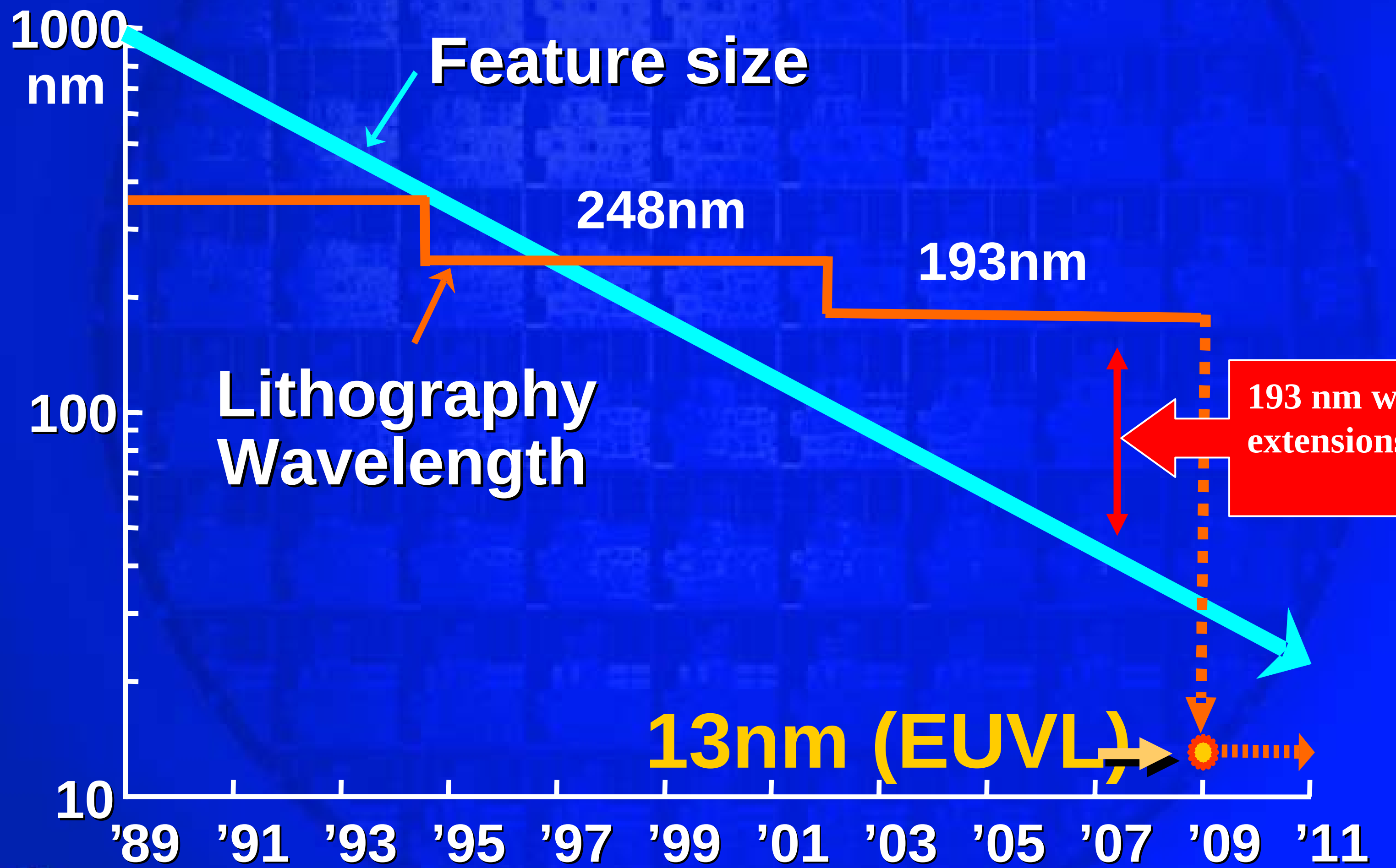
Lithography Challenge
Feature size scaling faster than wavelength reduction



PSM used extensively in today's technology

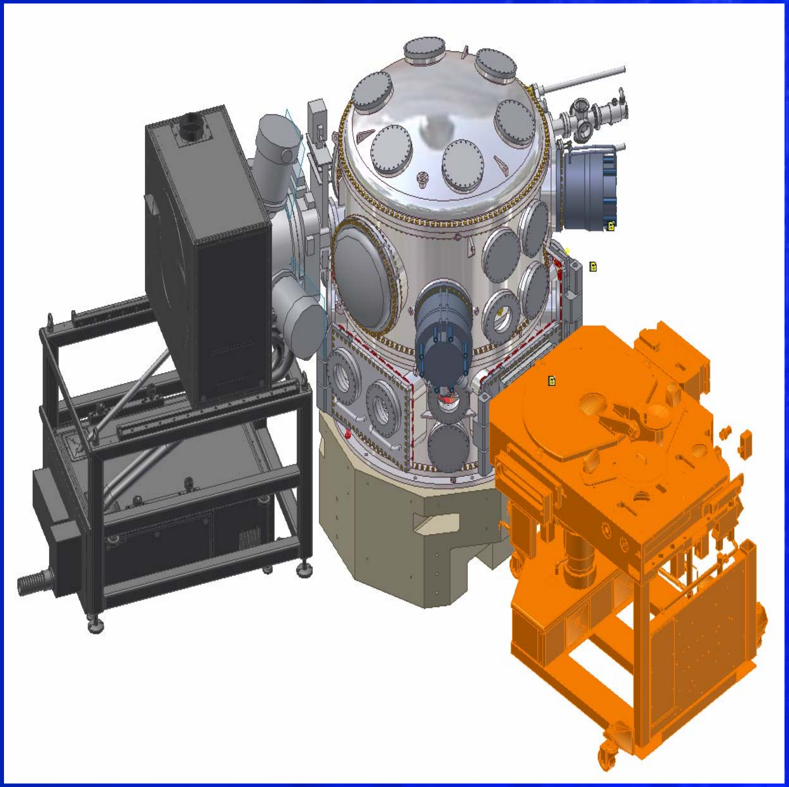
Intel's Strategy

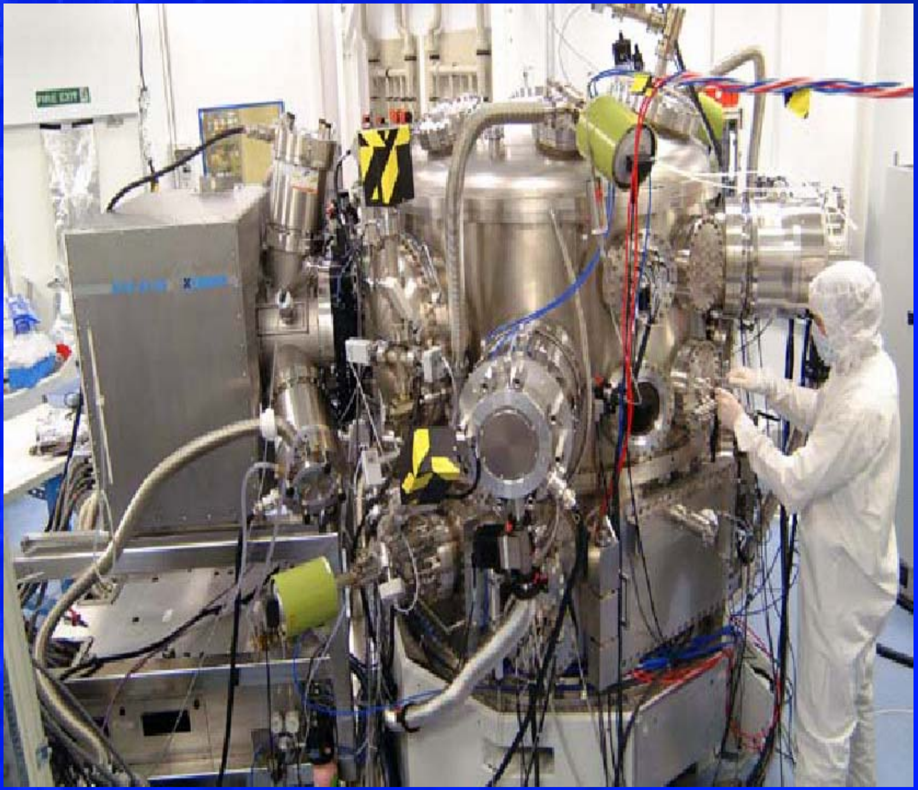
- Employ 193 nm lithography until EUV is available
  - Enabled by development of advanced OPC and PSM strategies
- Use EUV for P1268, if tools are available and affordable
  - Backup is 193 nm with extensions
- Continue to monitor all emerging lithography technologies

EUV Progress

- The EUV LLC demonstrated proof of concept imaging using the Engineering Test Stand
- Intel is installing an EUV microexposure tool and mask making tools to expand internal research activity.
- Intel actively works with universities, suppliers and SEMATECH to help develop infrastructure for reticle handling, masks, sources, and resist.

Intel EUV Micro-Exposure Research Tool



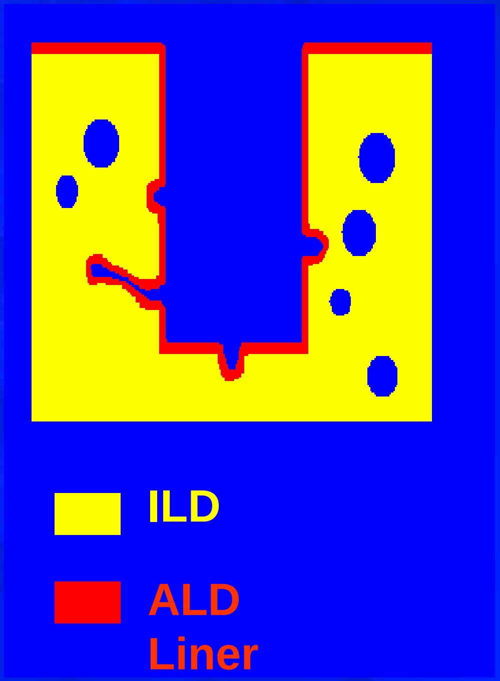


Delivery: Complete Q1 '04

Optics: 5X, 0.30 NA

Ultra Low K integration

- **Highly porous materials are required for ultra low dielectric constant (k<2.0)**
  - **ALD process will coat internal surfaces of porous films causing electrical leakage**
  - **Film needs to be compatible with CMP and packaging**



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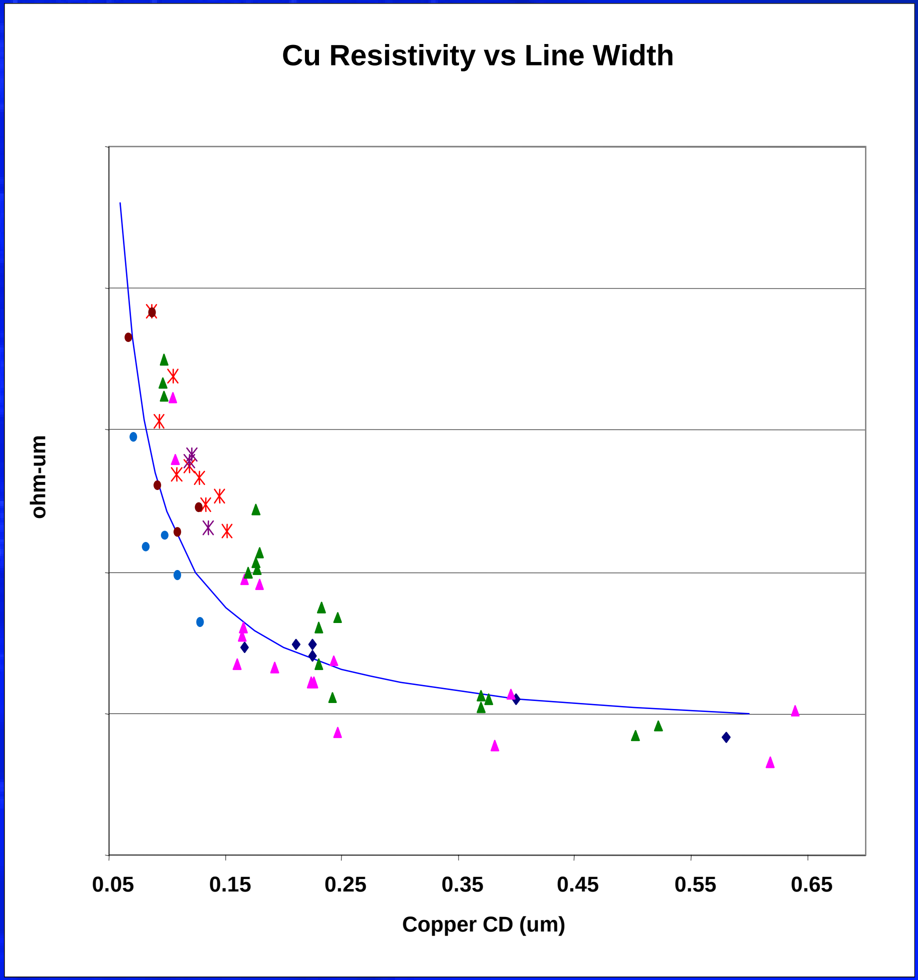
Metal Resistivity

- **Resistivity is a growing concern as interconnects scale.**
- **Electron scattering causes exponential rise as feature size approaches electron mean free path .**



New Materials, Devices Extend Si Scaling

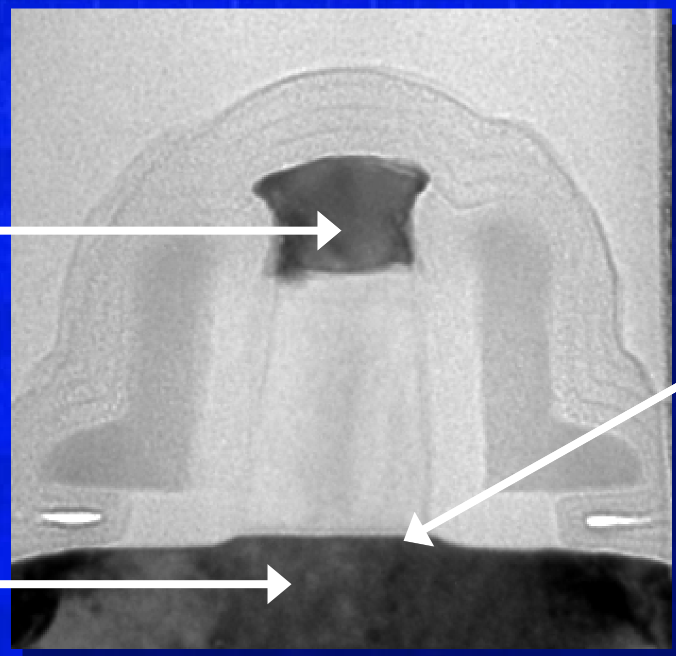
Changes Made

Gate

Silicide added

Channel

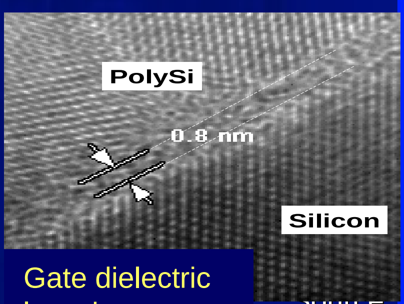
Strained silicon



Transistor

Future Options

High-k gate dielectric



Gate dielectric less than 3 atomic layers thick

Source: Intel

Source: Intel

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Materials Innovation Extends Si Scaling

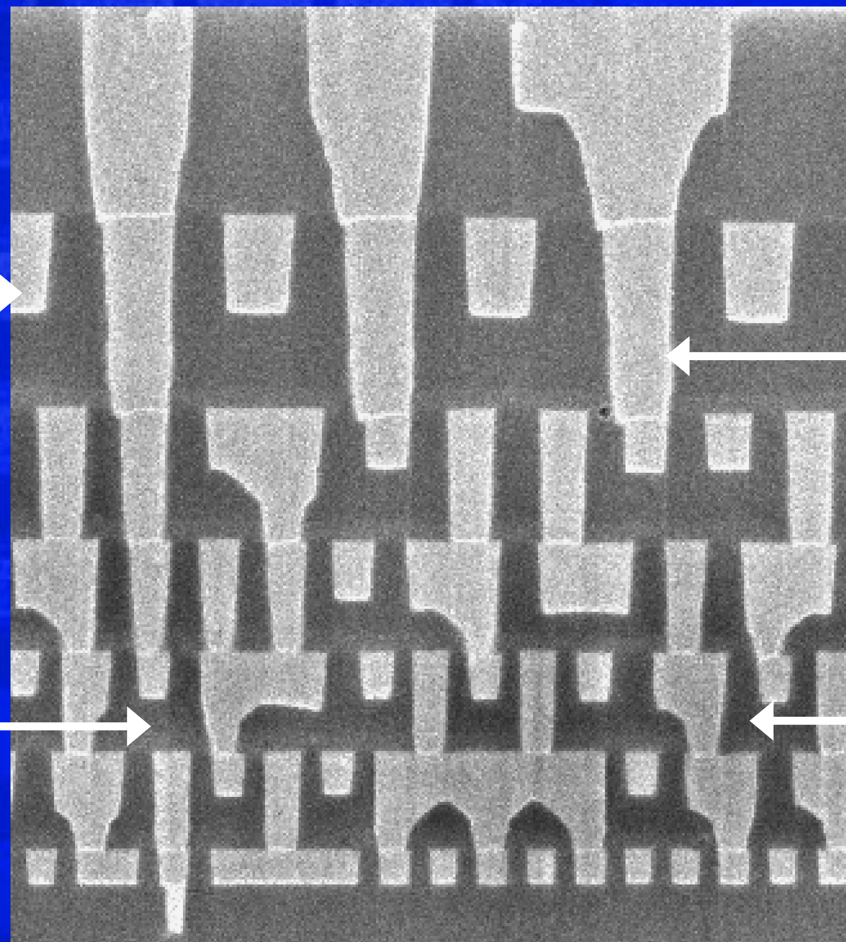
Changes Made

Metal lines

Al → Cu

Insulating dielectric

SiO_2 → SiOF → CDO (low-k)



Interconnects

Source: Intel

Future Options

New Thinner Barrier Layers

Ultra Low-k Dielectric

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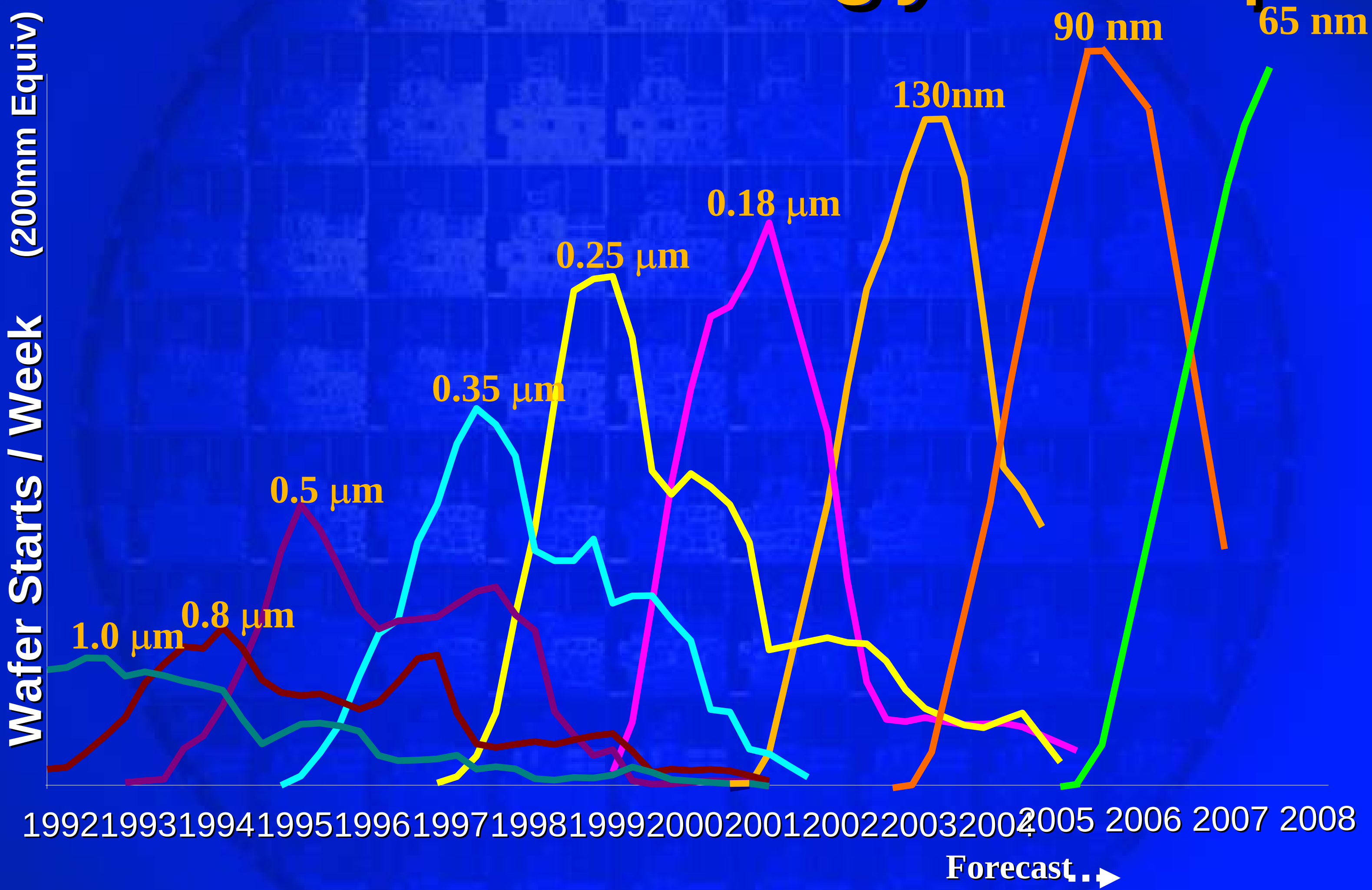
Intel's Silicon (Logic) Technology Roadmap Progress/Phases

	P1262	P1264	P1266	P1268	P1270
'Technology Node' (nm)	90	65	45	32	22
Research (internal) starts	Done	Done	Done	Started	2005
Pathfinding starts	Done	Done	Done	2005	2007
Development starts	Done	Done	2005	2007	2009
Ramp (Introduction)	Done	2005	2007	2009	2011

Evolution of Intel Technology

Node	P856 0.25µm	P858 0.18 µm	PX60 130nm	P1262 90nm	P1264 65nm	P1266 45nm	P1268 32nm
Metal	Al	→	Cu	→	→	→	→
ILD	SiO_2	SiOF	→	SiOC	→	→	?
Gate Oxide	SiO_2	→	→	→	→	Hi k	→
Gate Electrode	Poly	→	→	→	→	Metal	→
Channel	Si	→	→	Strained Si	→	Trigate?	?
Litho (nm)	248	→	→	193	→	→	EUV (preferred)

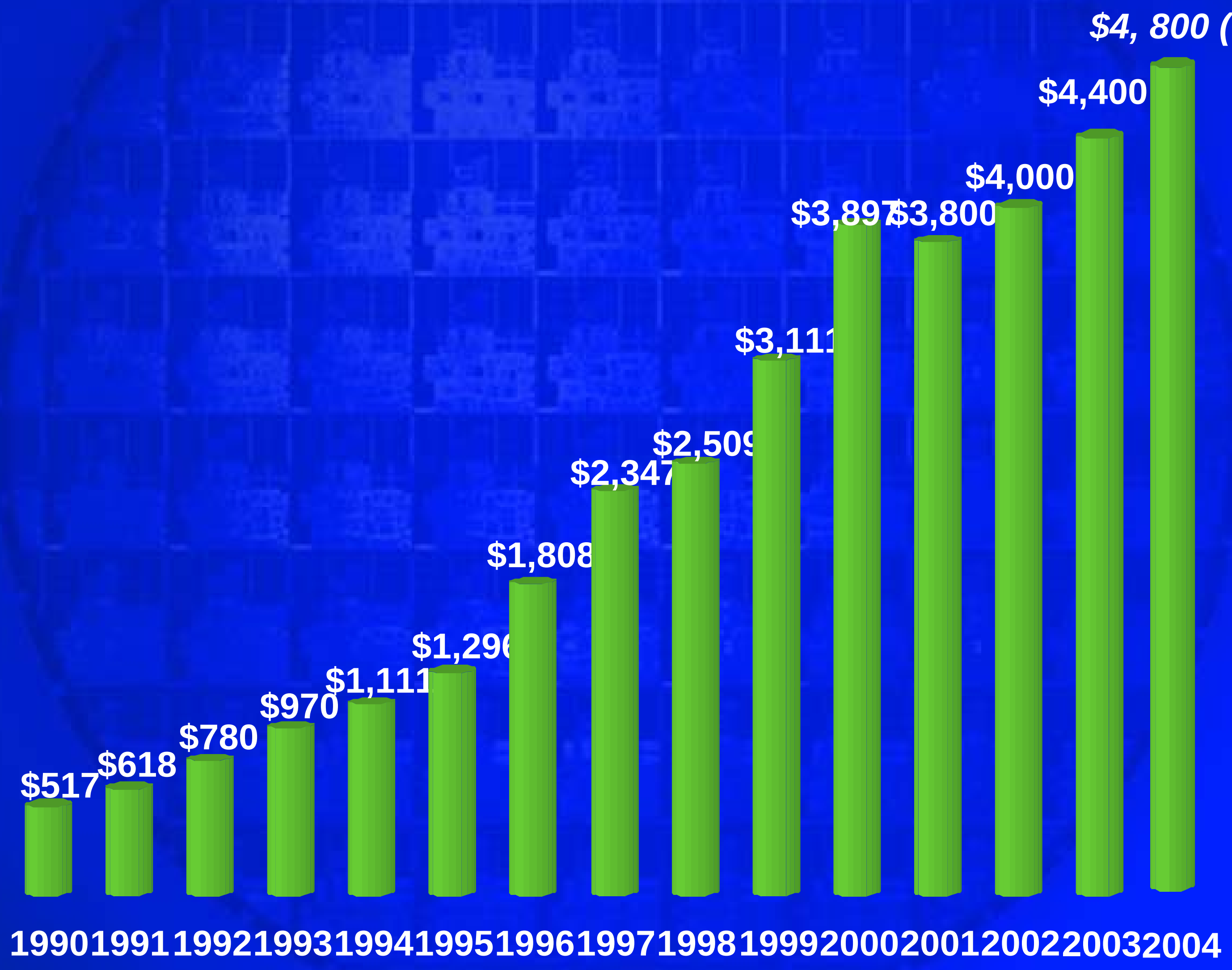
Intel Technology Ramps



New Technology Ramps Every 2 Years

How Does Intel Operate in this Environment?

Intel R&D Investment ($M)



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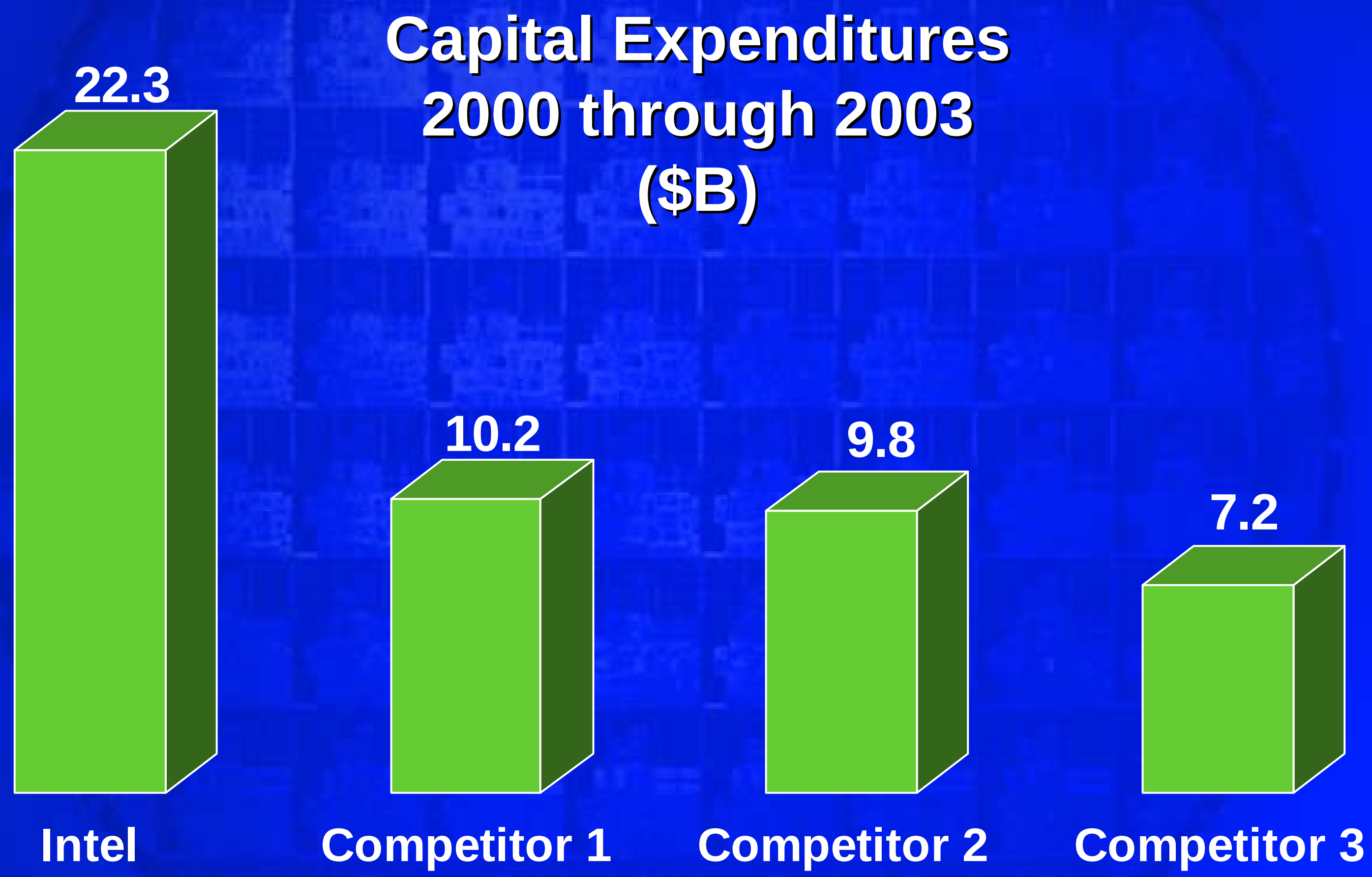
Source: Intel Annual Report

Intel Capital Expenses



Technology Focus: Microprocessor Products

- Research Groups are de-centralized
  - Aligned with Development groups.
- Central Technology Development groups
  - Logic: Hillsboro, Oregon
  - Memory: Santa Clara, California
  - Packaging: Chandler, Arizona
- Copy Exactly! from Development into Manufacturing
  - Enables Steep HVM Ramp

Production, Development and Research Synergy

F20: 200mm
130 nm Production

D1C: 300mm,
130nm Production
90nm Development

RP1: 300mm
Research

D1D: 300mm
65 nm Development

Worldwide Intel R&D Presence

75+ labs and over 7,000 R&D professionals

Decentralized Approach Fosters Innovation

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The Technology Funnel

Pre 32 nm

External Research
disruptive ideas
learning

32 nm

Internal research

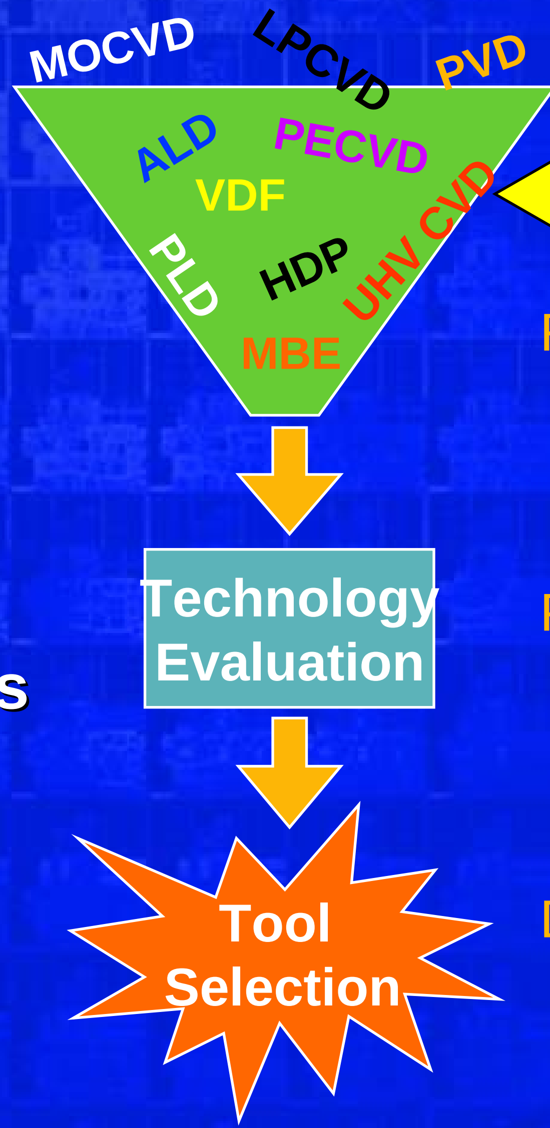
disruptive modules

45 nm

Integrate/select options

65nm

Optimize technology



Supplier/University engagement begins here!

Research

Pathfinding

Development

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Alignment with Intel Roadmap

- Increasing complexity drives greater number of technology options
  - Novel materials, tools
- More options means R & D dollars must be spent wisely
  - Increased risk, opportunity
- Staying aligned with Intel's roadmap helps to ensure that R & D funds are focused on correct priorities

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Supplier Expectations

- Manufacturing excellence
  - Timely, cost-efficient support during HVM ramp
  - Quality systems
- Advanced Development
  - New equipment and capabilities matched with Intel's roadmap
  - Process Development
- Research
  - Collaborative efforts to foster innovation

Summary

- **Moore's Law has enabled computing /communication convergence and is enabling computer /communication /consumer convergence.**
- **Scaling challenges will be met through rapid introduction of new tools, materials and architectures.**
- **Challenges will be met only through unprecedented collaborative effort between IC manufacturers, suppliers and universities**

For further information on Intel's silicon technology and Moore’s Law, please visit the Silicon Showcase at www.intel.com/research/silicon